

Design Review2

A Method to Implement Low Energy Read Operations, and Single Cycle Write After Read in Subthreshold SRAMs

by

The Sub-threshold Team
Author
Arijit Banerjee

TABLE OF CONTENTS

Chapter 1	Summaries of Publications beyond those from the Proposal	2-4
Chapter 2	Printouts of Simulation Figures and Corresponding Schematics	5-16
Chapter 3	Results	17-20
Chapter 4	Group's Progress and Remaining Tasks	21-22
Chapter 5	References	23

Chapter 1

Summaries of Publications beyond those from the Proposal

Summaries of papers beyond those from the proposal:

In [7], authors proposed a disturb mitigation scheme which claimed to achieve low power and low voltage operation for SRAMs in deep submicron technology. The proposed scheme is reported to involve a floating bitline technique and a low-swing bitline driver. They claimed to achieve decrease in active power by 33% and 32% respectively at the FF corner. They also reported achieving 47% and 60% active power reduction at CC and SS corners with this method. The proposed scheme is claimed to be 35% better in active energy saving than that of the conventional writeback scheme.

In [8], authors proposed a bitline amplitude limiting scheme which is reported to achieve 26% total energy reduction at 0.5V with 7% of penalty in speed, and less than 2% in the area penalty. This method involves a bitline amplitude limiter which is capable of reducing dynamic energy by suppressing the excess bitline amplitude. It was claimed to be reduced the leakage automatically too. With the simulated results they reported 20% and 29% reduction in dynamic energy and leakage energy. The circuit was claimed to be implemented in 40nm technology with measured 19% energy reduction with the proposed method.

In [9], authors proposed a novel architecture for the reduction of dynamic and static power consumption in SRAMs. The method involves the segmented virtual grounding of the SRAM cells with leakage reduction by increasing the threshold voltage of the transistors using body bias. The write and read energy is reportedly being decreased by decreasing the bitline voltage swing. This scheme is claimed to reduce the read and write energy consumption by 44% and 84% respectively in 130nm CMOS technology. They also reported 15X leakage reduction compared to the conventional scheme.

In [10], authors proposed circuit techniques that can reduce the energy consumption in SRAMs without scaling the supply voltage. They proposed an energy efficient hierarchical bitline scheme saving energy consumption used for bitline precharge. They also proposed an energy efficient offset-cancelling circuit and a robust timing generation circuit from process variability standpoint. The proposed circuits are claimed to be implemented in 28nm as 4Mb SRAM with 7% penalty in area. The dynamic energy reduction of 60% and leakage energy reduction of 10% are reported in this paper with these schemes.

In [11], authors described a scheme of dynamic voltage and frequency control for a 256x64 SRAM macro to reduce the energy in active and standby mode. The method is claimed to monitor the external clock and varies the supply voltage and the body bias to achieve reductions in energy. The method is reportedly achieved 83.4% and 86.7% energy reduction in active and standby mode respectively. The authors also proposed an energy replica method to monitor the energy of the subsystem with their scheme described earlier.

Findings from the prior works:

In [1], from the Fig. 8 (a) of the [1] shows that the Monte Carlo (MC) data indicating “mean-3sigma” RSNM of ST is lying in between 50mV to 0mV and “mean – 3sigma” hold signal to noise margin (HSNM) lying nearby 100mV. On the other hand in Fig. 9 the “mean + 3sigma” V_{min} looks like lying in between 350-400mV. Hence, from the process variation and robustness standpoint with 400mV of supply voltage the 3sigma worse case values indicate that there may be failures in the bitcell in below 350mV if fabricated.

In [2], from the Fig. 7 it can be seen that the 3sigma worst case Read and Hold SNM is not robust at all. With 300 mV supply the “mean – 3sigma” WSNM is around 100mV, and “mean + 3sigma” Hold SNM is about 85mV, and “mean – 3sigma” read SNM becomes negative.

In [5], the Fig. 6, 7, 8 and 9 shows RSNM distributions of the proposed bitcell versus standard 6T bitcell. It can be referred from the plots that at 400mV the worst case “mean – 3Sigma” RSNM is around 20mV, and due to this fact there can be read failures from the standpoint of process variation.

Our observation from studying the papers [1] to [6] is that below 400mV most of the published SRAM bitcells are having issues with robustness standpoint limited by the bitcells’ worse case RSNM, VDRV, RSNM, HSNM, V_{MIN} perspective which may lead to failures if the supply voltage is lowered further in subthreshold domain. Hence, lowering dynamic energy consumption in SRAM by lowering supply voltage is been hindered by the poor robustness in below 400mV supply voltage in SRAM bitcells. Hence, we try to research other ways to mitigate energy consumption in sub-threshold SRAMs. The method mentioned in [3] as writeback is a common way to avoid the half select problem in subthreshold SRAMs.

The Proposal:

We propose a method to utilize the concept of writeback mentioned in [3] to implement low energy read operations. In our Method we implement 128bit intermediate latches in the global bitlines to latch all the 8 words (16 bits each) in a normal write after read (writeback), and read operation, and if the user reads from the same row in two or more consecutive read operation, the Read Word Line (RWL) does not toggle and we just read from the intermediate latches. With this scheme we investigate the dynamic energy savings by not switching RWL and row decoders in the low energy read operations in which operating components of the memory are 16 bit output flip-flop, 128 to 16 bit bus interface logic, and input flip-flops only. We also plan to compare the results of [7] to [11] with this work in the final project report.

Motivation:

There was a version of sub-threshold data memory used in UVa Body Sensor Network (BSN) chip last year 2011. The memory had normal 128 bits of DIN and DOUTs directly providing to the user with

operating voltage of 0.5 volt and frequency of 200 kHz. In the memory the writing operation was done in effective two cycles by write after read approach which is standard in sub-threshold memories to avoid the half select issue. Recently the BSN chip team has changed the BSN Instruction Set Architecture (ISA) along with the bus width of the main data and address bus to 16 bit each, and they demanded new features in the memory like somehow single cycle effectively writing, lowering the read dynamic power dissipation, and other features like including input and output flops, converting the existing 128bit bus to 16 bit bus interface to the SOC, and so on. In order to meet their requirements we added new circuits and modified the Data memory to meet the specification.

Design component, research component and simulations for the projects:

We tabulated the regular design components, research components and simulations to be done for the project as follows provided that we had started with BSN chip 4KB SRAM to improve over Energy metrics:

	Regular Design Component	Research Component	Simulations to be done for The Project
i)	128bit to 16bit bus interface logic	Low Energy Read	Normal Read , and Single Cycle Write After Read for functionality
ii)	Pulse generator for Single Cycle Write after Read	Single Cycle Write After Read	Low Energy Read and Normal Read simulations for energy comparison for 0.5v, 0.4v, 0.3v and one superthreshold voltage 0.9v for energy trend comparison
iii)	Comparator/Statemachine for Low Energy Support		Each individual New Components' Functionality Check
iv)	Intermediate Latches for Low Energy Read and Single Cycle Write after Read		

Chapter 2

Printouts of Simulation Figures and Corresponding Schematics

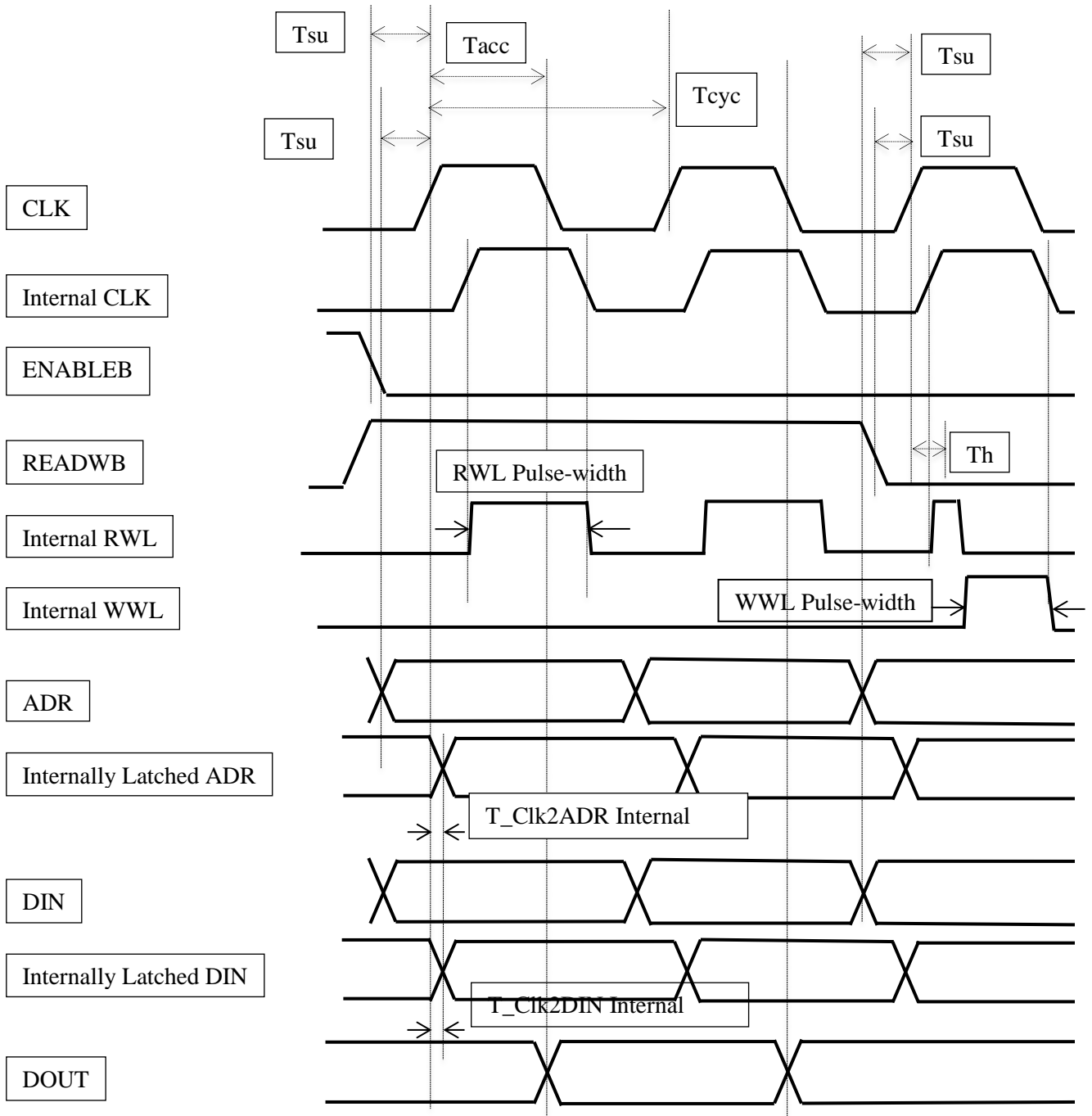
For the proof of concept we provide the suggested pin description table, and timing diagrams taken from “SRAM Specification Document November Test Chip 2012.doc” from BSN chip team followed by actual schematic and simulation figures from the next page. Rest of this page is intentionally left blank for formatting. The pins correspond to the low Energy Read operations of the memory in the pin description table are BURSTENB and BURST_RESET and the mode is called “BURST” in the SRAM Memory Specification Document.

Pin Description Table for the DATA Memory:

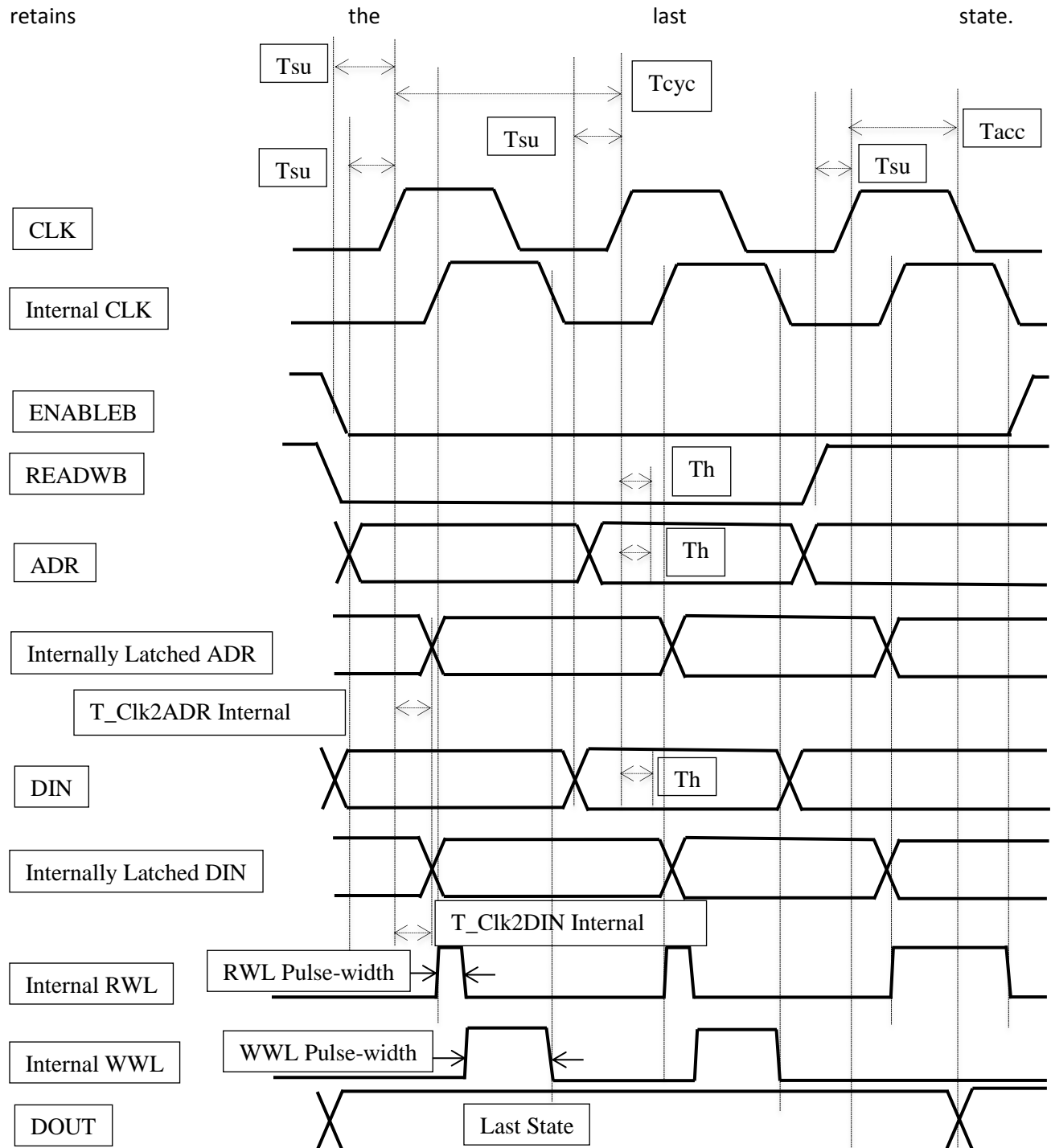
Pin Name	Pin Description	Latching Edge
Input Pins	All the input pins are having their own flops in the memories and they are latched in the pos-edge of the external clock (expection- BURST_RESET is asych)	
CLK	latched on the rising edge of the clock, output data is latched on the falling edge of the clock	
DIN<0:15>	DIN stands for data input bus pins, and should be asserted 1 or 0 before the clk positive edge accordingly, given a setup time is provided.	Pos Edge
ADR<0:10>	ADR stands for address bus pins. Should be asserted 1 or 0 before the clk positive edge accordingly, given a setup time is provided.	Pos Edge
ENABLEB	ENABLEB is a active low clock gating pin for the SRAM. In case of asserted to 0, it allows the SRAM to operate else it gates the clock and stops all read or write operation, but the internal content of the memory remains valid.	Pos Edge
READWB	READWB is the pin for selecting an read or write operation. If asserted 1, it allows the read operation. In case of asserting the same to 0, it allows write operation.	Pos Edge
EN<0:3>	EN is an active low power gating pin for each of the SRAM banks. 4KB memories will have 4 banks (EN<0:3>), 2KB memories will have 2 banks (EN<0:1>). If no banks are active, then the periphery is automatically power gated.	Pos Edge
WR<0:2>	WR stands for write after read delay control pin, and should be asserted proper 3 bit value before the positive edge of the clock accordingly, given a setup time is provided.	Pos Edge
BURSTENB	BURSTENB is an active low pin, allowing for burst enable read operations. Setting this pin high will disable burst mode reads, allowing us to compare the energy savings of using burst enable	Pos Edge
BURST_RESET	BURST_RESET is an asynchronus reset pin, which will be responsible for resetting the burst enable register. This will ensure that the first read operation after power up does not use the burst enable mode. This signal will be controlled by the global reset signal	Asynch

Pin Name	Pin Description	Latching Edge
Output Pins		
DOUT<0:15>	DOUT stands for data output bus pins. The data is latched on the negative edge of the clock and remains valid until the next negative clock edge.	Neg Edge

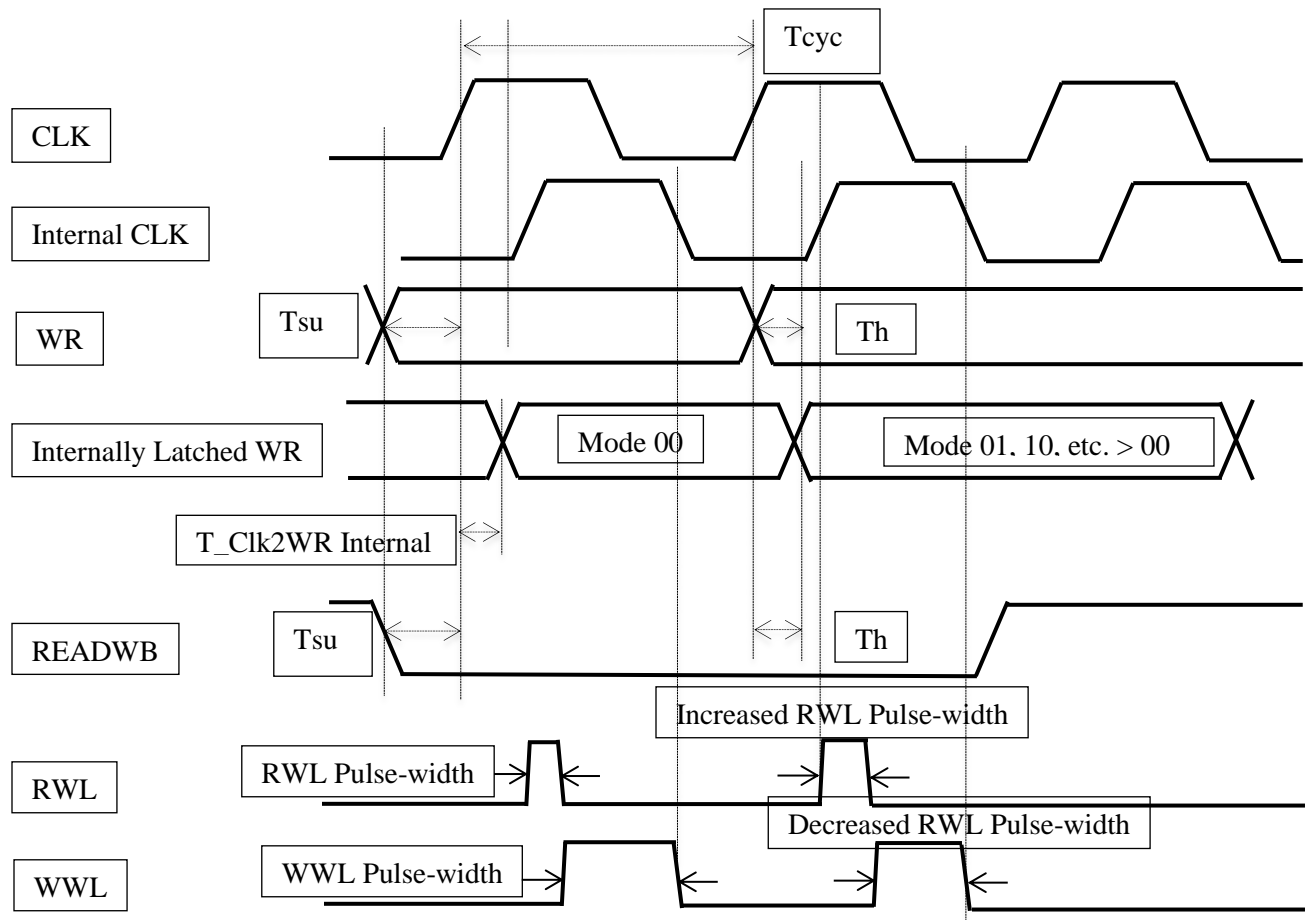
Timing Diagrams for Read Operation: The timing diagram provided represents two consecutive read operations and a write operation. Other internal signals like internal clock, internally latched DIN and ADR signal, and read word line (RWL) and write word line (WWL) are also specified for clarity. [Here T_{su} is setup time, T_{acc} is access time T_{cyc} is cycle time and T_h is hold time for all timing diagrams.]



Timing Diagrams for Write after Read Operation: The timing diagram provided below represents two consecutive write after read operations and a read operation. Signals like internal clock, read word line (RWL) and write word line (WWL) are also specified. In the write after read operation the output bus retains



Internal Change of Waveforms for WR value change: The timing diagram below describes how the RWL and WWL pulse widths changes with respect to change in WR modes. We can see that setting a higher WR mode will increase the RWL pulse width at the cost of decrease in the WWL pulse width.



Annotated full schematic of 4KB subthreshold SRAM data memory:

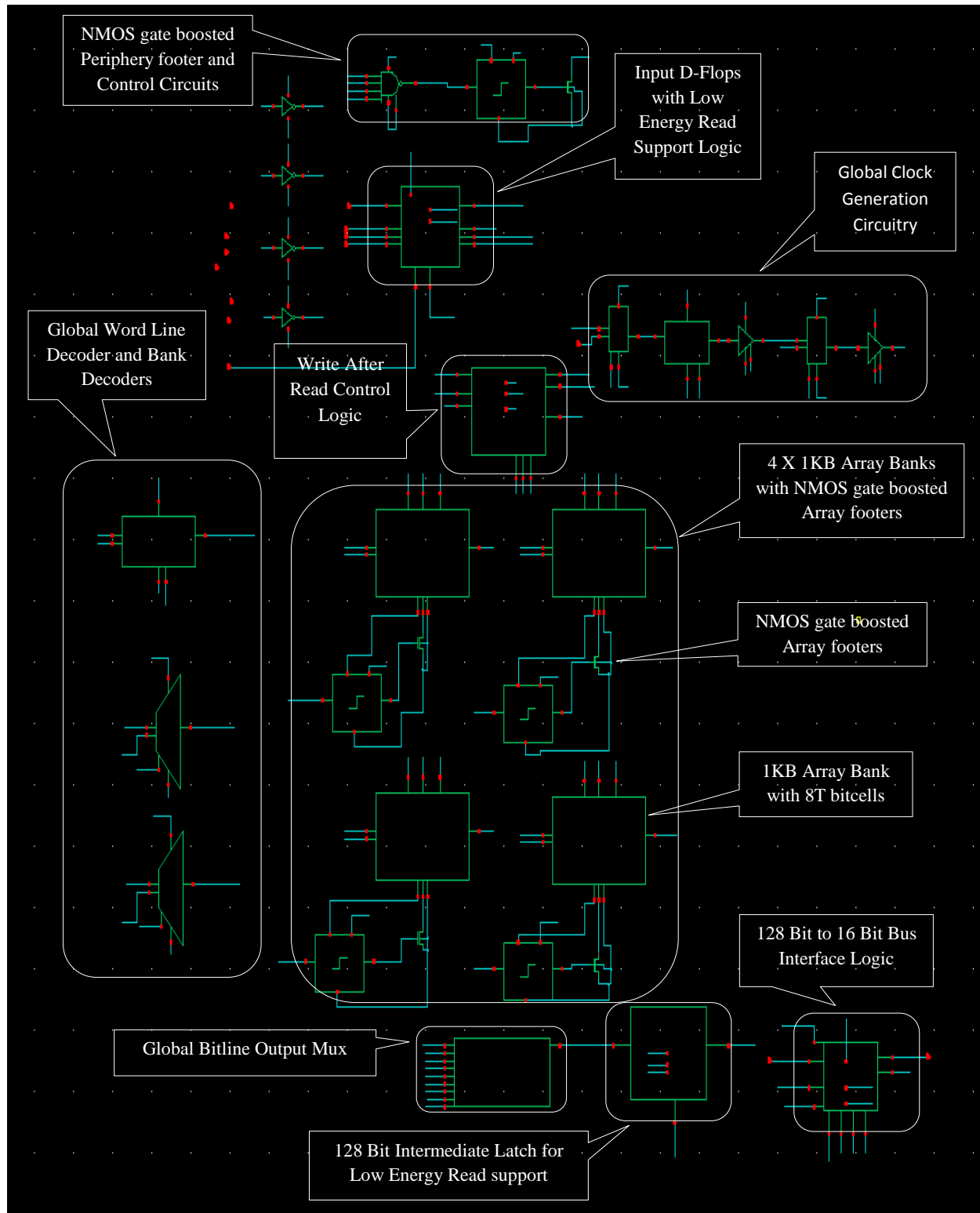


Fig. 1-a

Simulated and annotated waveform of the single cycle write after read, and normal read operations:

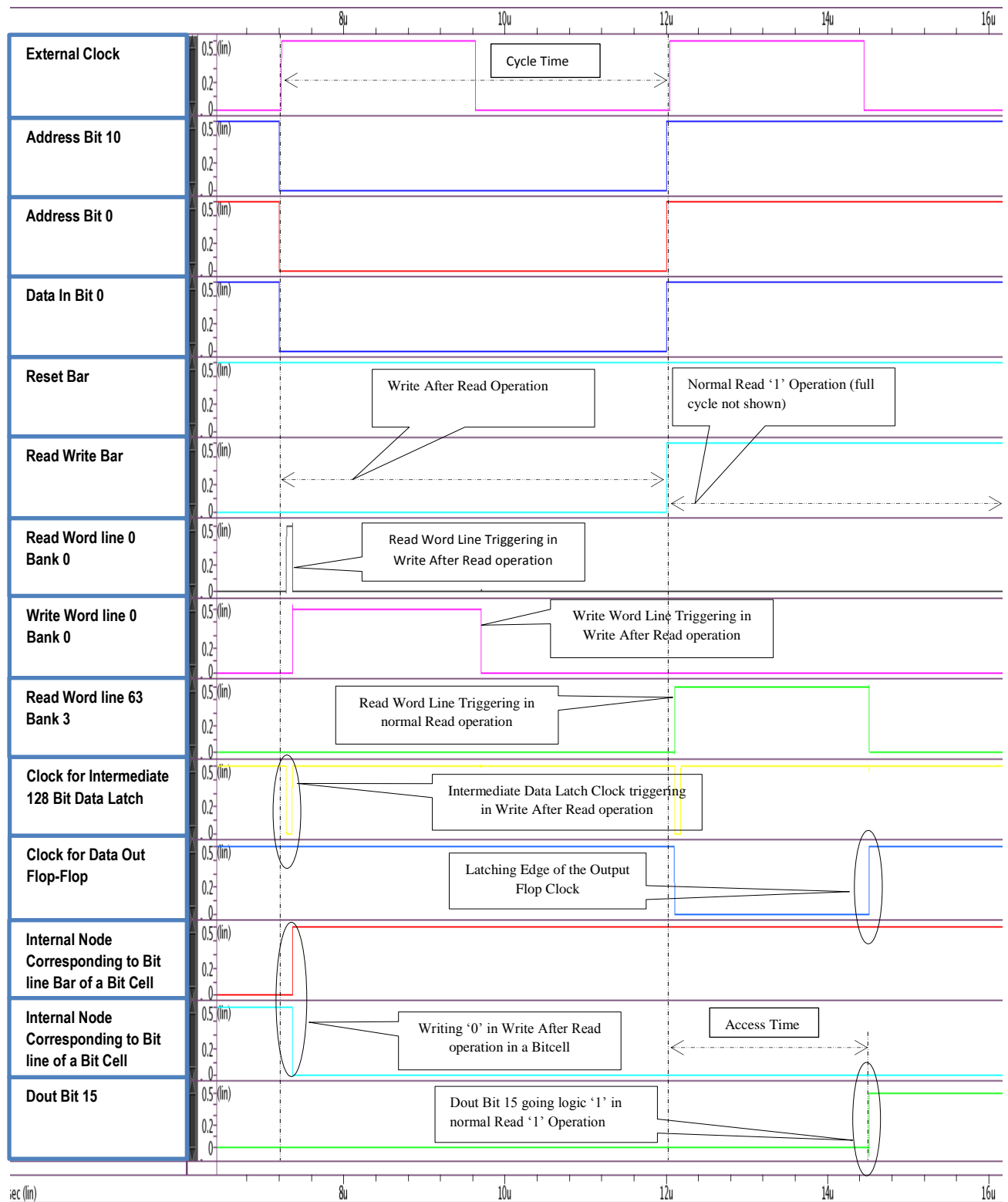


Fig. 1-b

Simulated and annotated waveform of the low energy read operations:

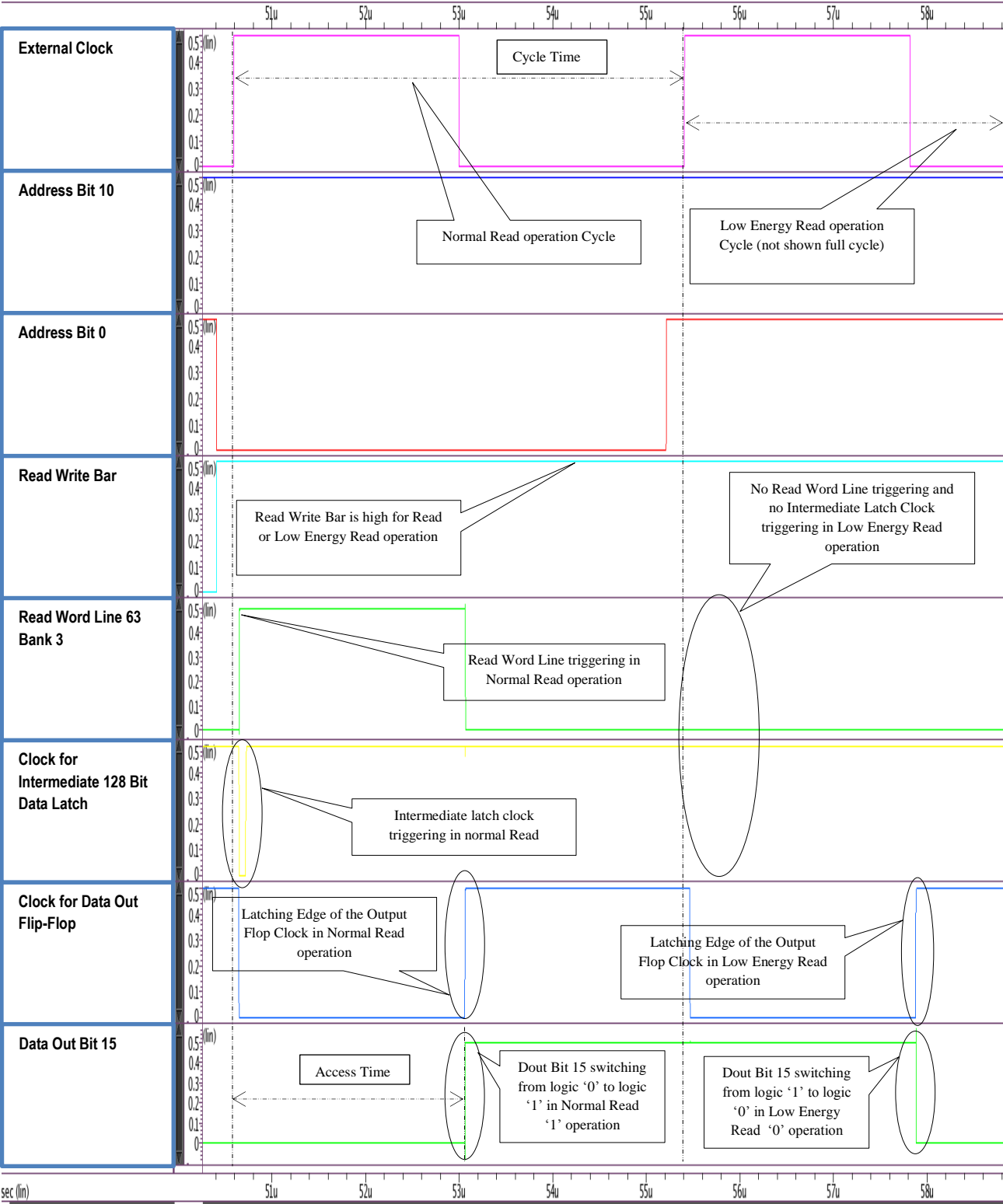


Fig. 1-c

Simulated and annotated waveform of the low energy read operations for energy measurement:

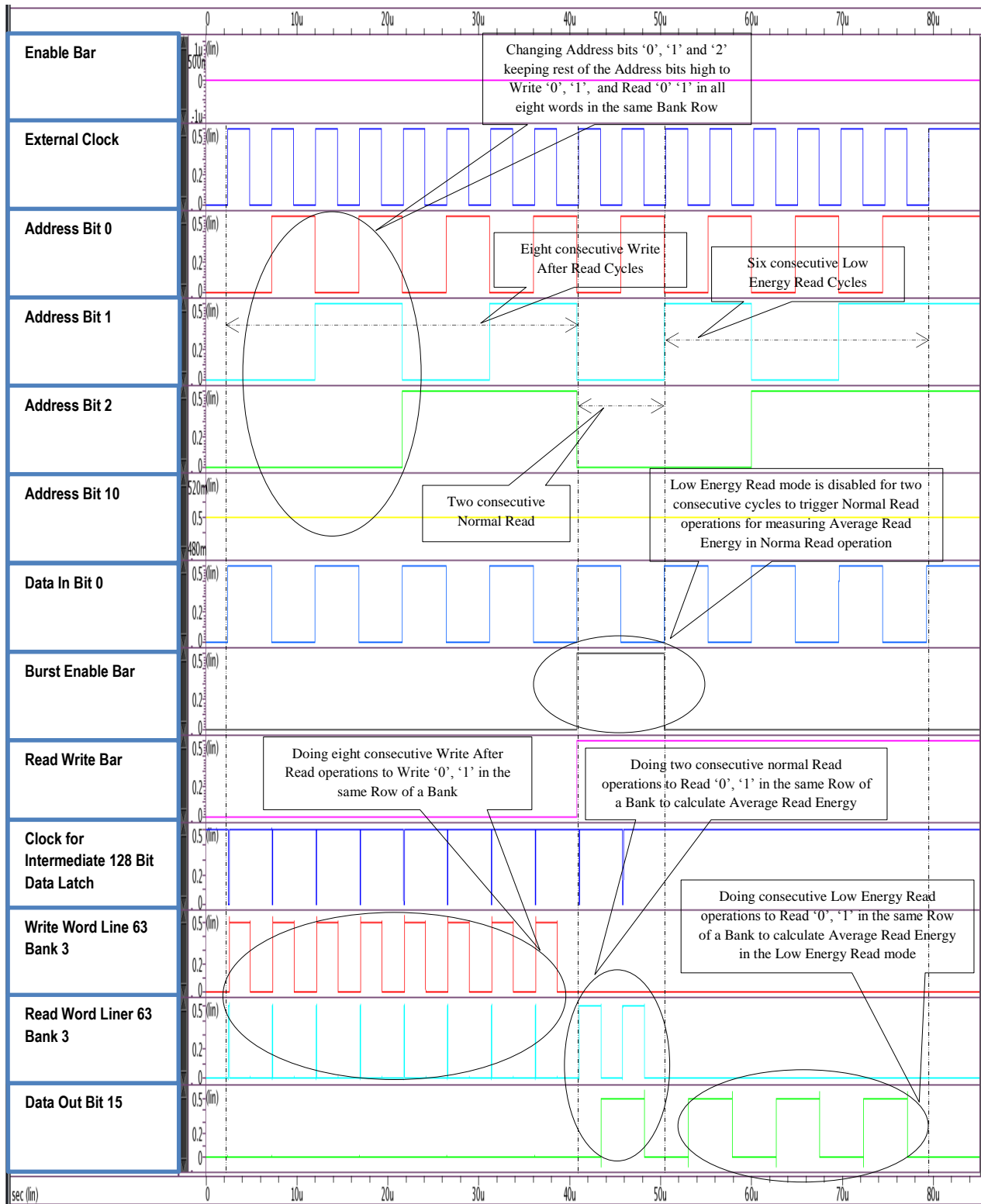


Fig. 1-d

Annotated schematic for low energy read operation support in 4KB subthreshold SRAM data memory :

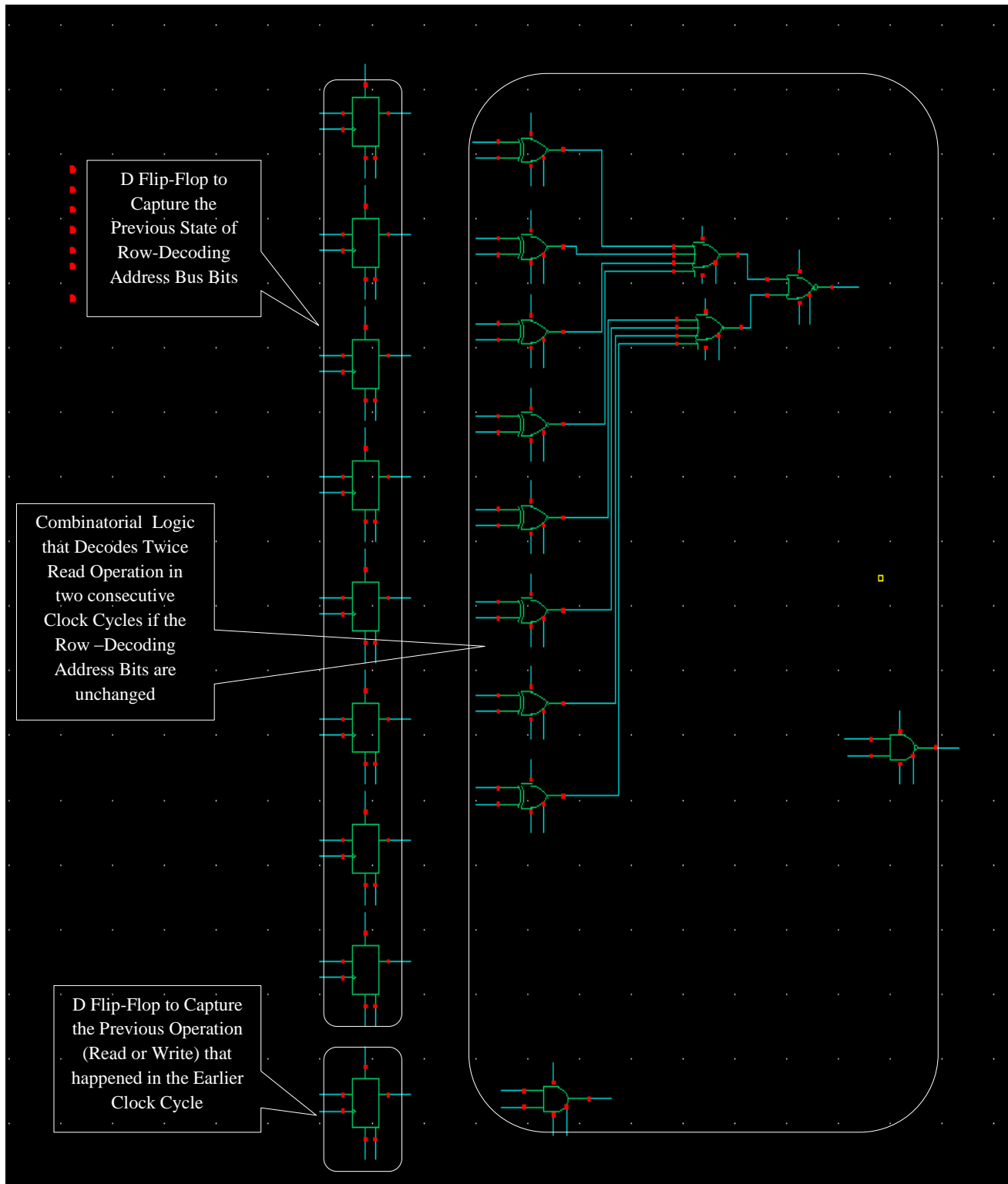


Fig. 2

Annotated schematic for single cycle write after read control logic, output-flop, and 128 bit intermediate latch clock generation logic in 4KB subthreshold SRAM data memory:

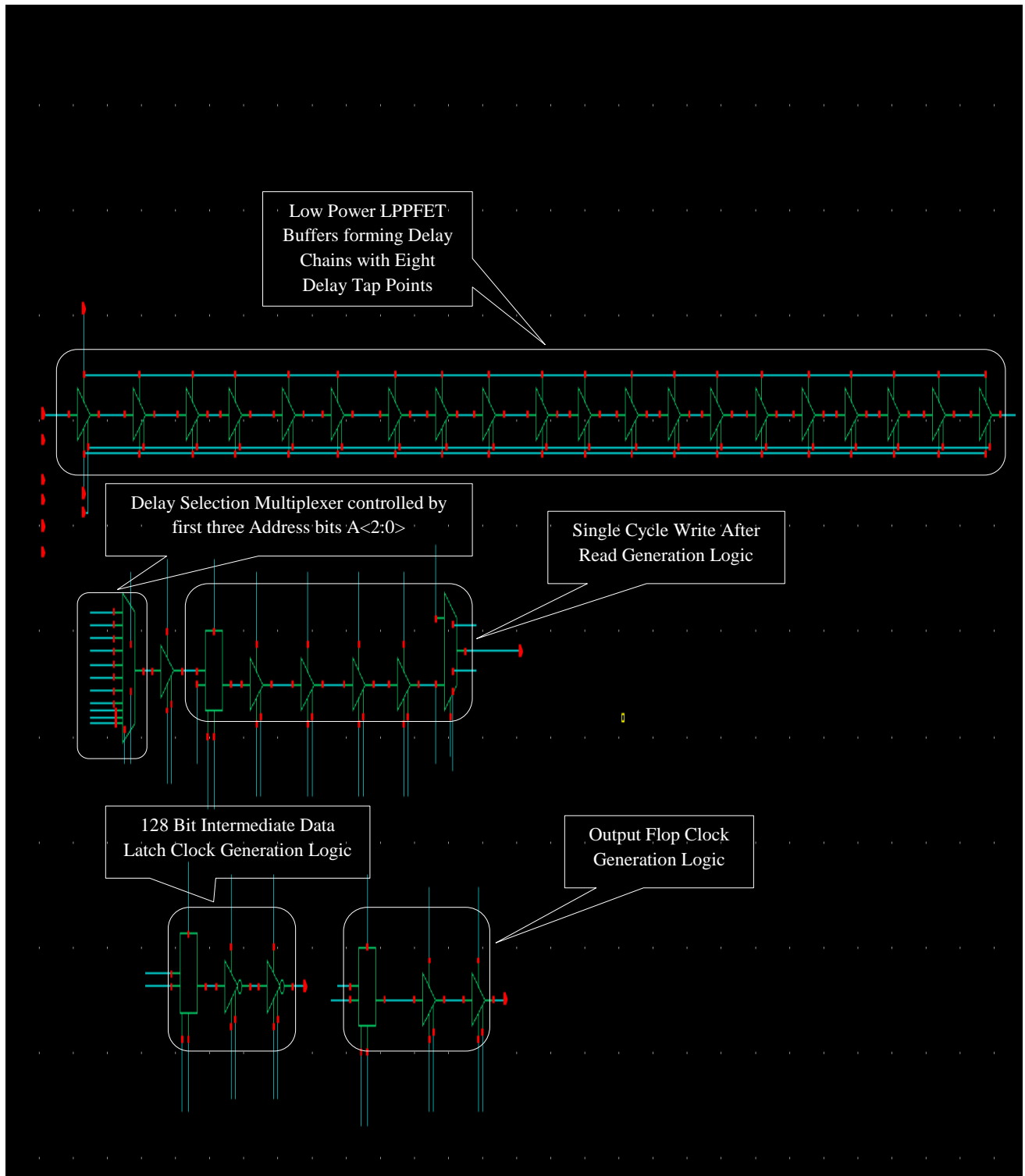


Fig. 3

16 bit bus controller and 128-to-16bit bus interface logic:

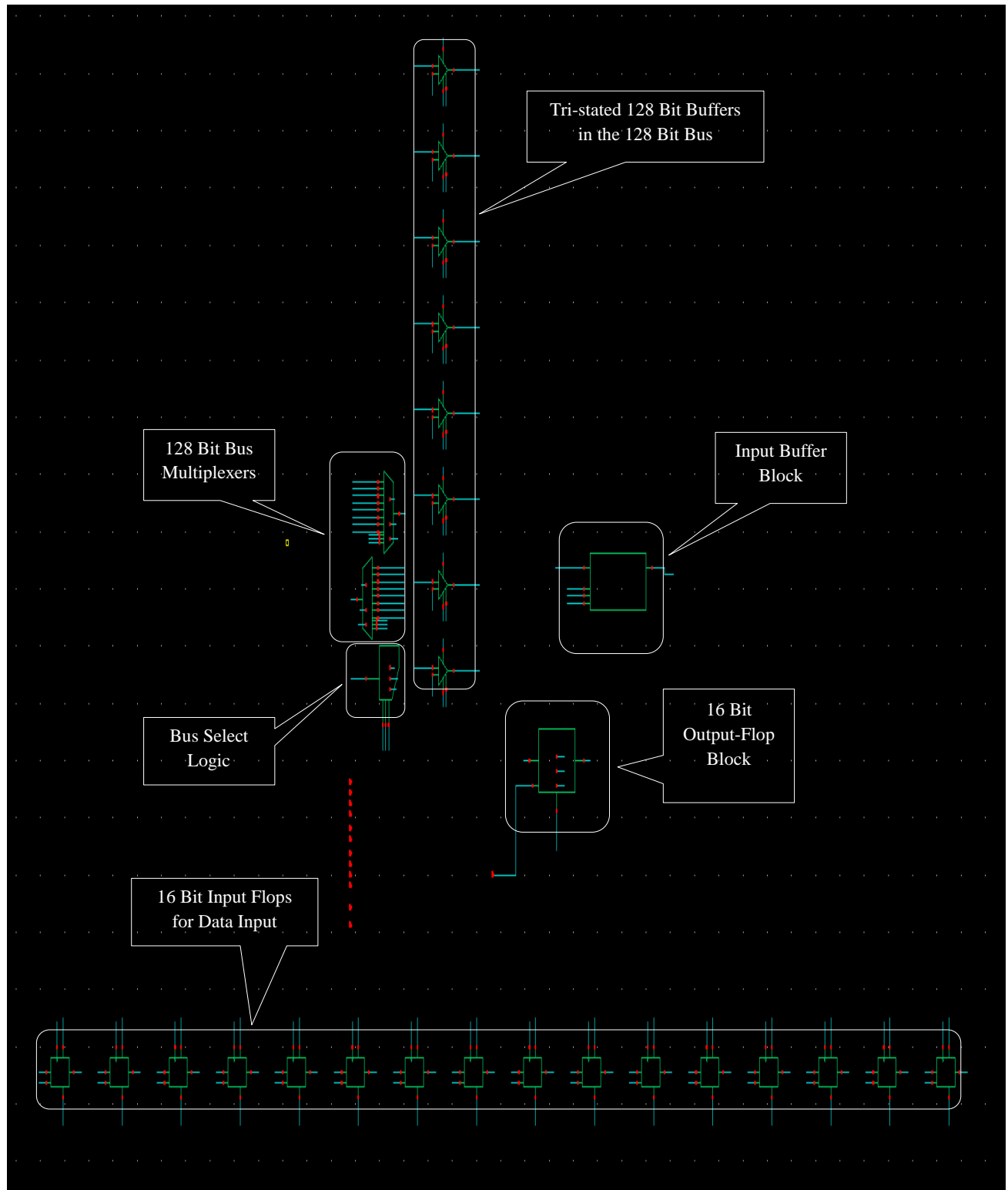


Fig. 4

Chapter 3

Results

We simulated the low energy read operations preceded by the normal read operations in the new Design of 4KB Data Memory, and got the following table for energy savings or penalty in Joules. We used HSPICE with highest SPICE accuracy for all simulations (Below Data are all of 4KB Data Memory). [The term LER means Low Energy Read, and WAR means Write After Read. All currents are in Amperes]

Processes @ 0.5V 27C	(Old Design) Average Rd Energy	(New Design) Average Read Energy		(New Design) Average LER Energy	
			(New Design) Rd Energy Savings		(New Design) LER Energy Savings
TT	1.74E-12	1.73E-12	1X	2.47E-13	7X
FF	1.15E-12	1.85E-12	0.6X	2.86E-13	6.5X
SS	8.21E-13	1.47E-12	0.55X	2.42E-13	6X
FS	2.39E-12	2.26E-12	1.05X	3.07E-13	7.4X
SF	7.51E-13	1.34E-12	0.56X	2.34E-13	5.7X

Here we compared the sum of two cycle read and write energy of the old design with the write after read energy in new design and leakage penalty in new design as follows:

Processes @ 0.5V 27C	(Old Design) Average Wr + Average Rd Energy in two Cycle	(New Design) Average WAR or Wr Energy in one Cycle	(Old(Wr+Rd)/new(WAR) Energy Savings
TT	2.36E-12	1.48E-12	1.6X
FF	3.12E-12	1.51E-12	2X
SS	1.30E-12	1.60E-12	0.8X
FS	3.80E-12	1.53E-12	2.5X
SF	9.76E-13	1.28E-12	0.75X
Processes @ 0.5V 27C	(Old Design) Total Standby Leakage Current	(New Design) Total Standby Leakage Current	Leakage Savings
TT	7.05E-06	6.77E-06	1.04X
FF	2.27E-05	2.32E-05	0.97X
SS	2.55E-06	2.17E-06	1.17X
FS	1.23E-05	1.26E-05	0.98X
SF	6.90E-06	6.77E-06	1.01X

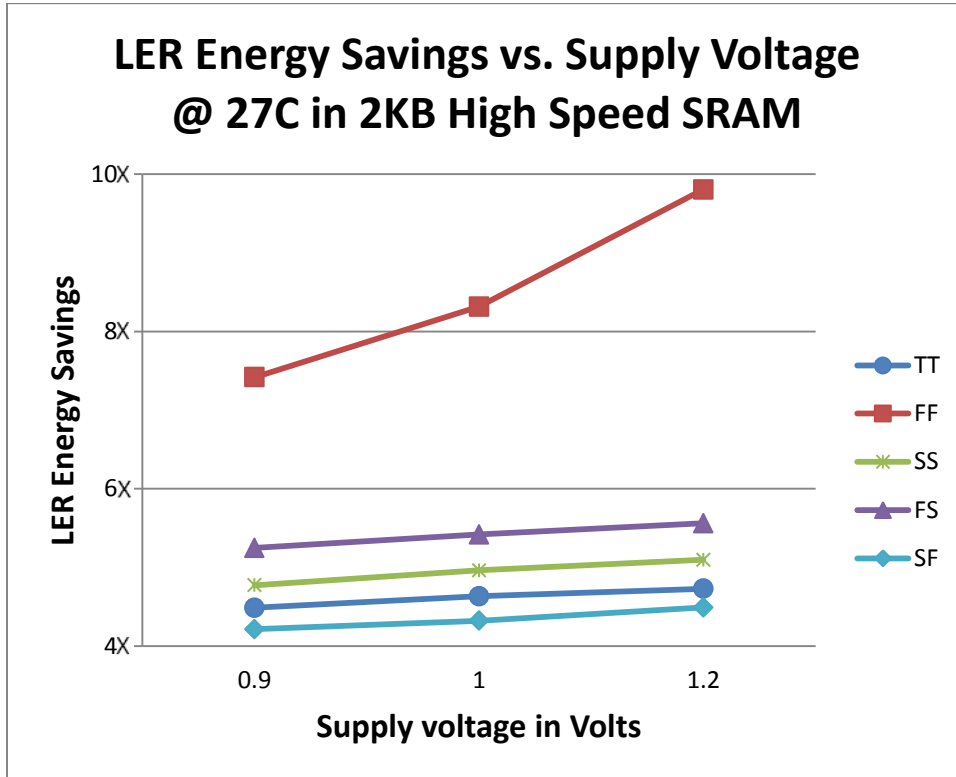
We also collected simulation data for Data Memory running with supply voltages 0.3V, 0.4V and found the below table of LER energy savings:

Processes	4KB Data Memory LER Energy Savings @ 0.5v 27C	4KB Data Memory LER Energy Savings @ 0.4v 27C	4KB Data Memory LER Energy Savings @ 0.3v 27C
TT	7X	4.6X	9.6X
FF	6.5X	3.6X	2.3X
SS	6X	2.8X	1.3X
FS	7.4X	1.7X	2.2X
SF	5.7X	4.5X	4X

We can see from the data that there is a trend of higher energy savings if we increase the supply voltage from 0.4V to 0.5V. The red marked data are either not complying with our expectations, or the memory has issues in those corners. We plan to investigate further in those cases to see a trend. In another memory of 2KB, named High Speed Memory designed with same components but having lesser banks and some changes in the timing path to operate correctly in higher voltages, we can definitely see a trend of higher LER energy savings if we increase the voltage in the table as follows:

Processes	2KB High Speed Memory LER Energy Savings 1.2v 27C	2KB High Speed Memory LER Energy Savings @ 1.0v 27C	2KB High Speed Memory LER Energy Savings @ 0.9v 27C
TT	4.7X	4.6X	4.5X
FF	9.8X	8.3X	7.4X
SS	5X	4.9X	4.8X
FS	5.6X	5.4X	5.2X
SF	4.5X	4.3X	4.2X

The trend for the LER energy savings is plotted below for the High Speed 2KB memory.



We can see that the FF corner is having higher LER energy savings than any other corner if the voltage is increased.

For the robustness of the Write After Read operation, we tabulated the read word line, write word line, and 128 Bit intermediate latch clock pulse widths in valid Read, and Write After Read operations for all WR<0:3> modes with all process corners, and marked failures in failed cases of functionality for Data Memory (DMEM) margin issues as follows:

Pulse Widths for DMEM (Base unit is in seconds)								
WR Mode	TT				FF			
Measured Parameters	RWL	WWL	128 Bit Latch	Tacc	RWL	WWL	128 Bit Latch	Tacc
000	92.2n	2.34u	90.1n	2.41u	failed	failed	failed	failed
001	227n	2.2u	225n	2.41u	27n	2.39u	26.2n	2.41u
010	293n	2.14u	291n	2.41u	35.6n	2.39u	34.8n	2.41u
011	368n	2.06u	366n	2.41u	43.6n	2.37u	42.8n	2.41u
100	451n	1.98u	449n	2.41u	52.6n	2.36u	51.9n	2.41u
101	514n	1.92u	512n	2.41u	60.8n	2.35u	60n	2.41u
110	610n	1.82u	608n	2.41u	73.3n	2.34u	72.5n	2.41u
111	721n	1.71u	719n	2.41u	85.1n	2.33u	84.3n	2.41u

Pulse Widths for DMEM (Base unit is in Seconds)								
WR Mode	SS				FS			
Measured Parameters	RWL	WWL	128 Bit Latch	Tacc	RWL	WWL	128 Bit Latch	Tacc
000	405n	1.92u	497n	2.42u	312n	2.09u	307n	2.42u
001	1.17u	1.25u	1.17u	2.42u	668n	1.73u	663n	2.42u
010	1.56u	864n	1.55u	2.42u	877n	1.52u	870n	2.42u
011	1.9u	524n	1.89u	2.42u	1.07u	1.33u	1.06u	2.42u
100	2.34u	85.1n	2.33u	2.42u	1.36u	1.04u	1.35u	2.42u
101	failed	failed	failed	failed	1.53u	866n	1.53u	2.42u
110	failed	failed	failed	failed	1.82u	576n	1.82u	2.42u
111	failed	failed	failed	failed	2.07u	326n	2.07u	2.42u

Pulse Width Data for DMEM (Base unit is in Seconds)				
WR Mode	SF			
Measured Parameters	RWL	WWL	128 Bit Latch	Tacc
000	73.9n	2.35u	72n	2.41u
001	214n	2.21u	212n	2.41u
010	292n	2.13u	290n	2.41u
011	356n	2.07u	354n	2.41u
100	430n	1.99u	428n	2.41u
101	488n	1.91u	487n	2.47u
110	598n	1.83u	597n	2.41u

From the measurement we can see that although some of the modes the Memory functionality is “failed” due to insufficient margin to generate read word line and write word line pulses correctly, there are plenty of modes in those the SRAM operates successfully. And we still keep the WR mode(s) in which one corner fails but TT corner passes as our target PVT for the design is TT_0.5V_27C.

Chapter 4

Group's Progress and Remaining Task breakdown for group members

We already completed the SRAM with all above mentioned sub-circuitry for low energy read operation support, single cycle write after read, 128 to 16 bit bus multiplexers, intermediate 128 bit latches and input and output flops. As this memory will always be operated at room temperature, we are simulating the same in 27C temperature only. We have simulated our sub-threshold memory in PVTs mentioned in the Timeline table including the PVT of TT_0.5V_27C, and we are getting the intended functionality from the simulations. The supply voltage of 0.5V was chosen by the BSN chip group as the supply for the digital logic used is 0.5v. The memory bitcell is already reported to work with the supply voltage near by the “mean +3 sigma” DRV Vmin of the bitcell which is nearly 350mV.

Below is the Timeline table showing the group's progress and remaining tasks in “Yellow” and “Red” color including the name of the owner of each task: Here one shared task, and two tasks are solely performed by BSN chip group member named Jim (James Boley) who is not a member of the VLSI 6332 “Subthreshold Group.”

	Tasks	Expected Completion	Status	Owner
1)	Schematic Implementation of Low Energy Read	9/7/2012	Done	Arijit
2)	Schematic Implementation of Single Cycle Write after Read	9/14/2012	Done	Arijit
3)	Measuring the Energy Saving in Low Energy Mode for in TT, FF, SS, SF and FS corners with 0.5v supply voltage	10/10/2012	Done	Arijit
4)	Checking Design Margins in TT, FF, SS, SF and FS for at least one WR mode	10/10/2012	Done	Arijit
5)	Building Layouts of each new component block	10/10/2012	Done	Arijit
6)	Integrating Layouts to Data Memory	10/30/2012	Done	Jim
7)	Running DRC and LVS over the full SRAM after Integration	10/30/2012	Done	Jim
8)	Extracting Lumped parasitics	TBD	Delayed	Arijit
9)	Simulate in TT, SS, FF corner with lumped parasitics	TBD	Delayed	Arijit
10)	Sign off and Tape out on February 2013	TBD	Delayed	Arijit & Jim
11)	Low Energy Read and Normal Read simulations for energy comparison for 0.5v, 0.4v, 0.3v and one superthreshold voltage 0.9v for energy trend comparison	11/14/2012	Done	Arijit
12)	HSIM vs. Spectre Simulation Comparison for Low Energy Read	11/23/2012	To Do	Arijit

We have faced challenges from various standpoints. As we are one student team, we have to put extra effort to complete the publication searching in IEEE, reading the publication thoroughly to select the useful ones, doing the sub tasks like simulations, schematic entry, layout entry, DRC and LVS of individual blocks, data generation, data collection, and analysis. We also faced challenges that the IBM 130nm RCX PDK was not compatible with Caliber 2009 version, which we already had, and we missed the deadline requesting and waiting to get the updated and IBM 130nm RCX PDK compatible 2011 version of the Calibre installed.

We have some direct questions related to “how to proceed?” in general as follows: How do you debug a trend in case a valid given trend of a particular circuit does not work in a couple of PVTs? How do you select a good publication from a pool of publications as a reference in your research? How do you organize your project and data, and manage time in order to execute the project in time? We believe these above questions always make us think more and more, and those are somehow related to the question of “how to proceed?”

From the timeline table we can see that we have maintained the planned tasks (1) to (7) and (11) in time meeting the deadlines, but we missed out the deadline of planned task (8) to (10) due to unavailability of one of the resource tools named Calibre release version of 2011 which is compatible to be used for extraction with the IBM 130nm updated XRC PDK. So, we think we have successfully maintained the timeline goals apart from those having resource issues.

Chapter 5

References

- [1] J. P. Kulkarni, K. Kim, and K. Roy, "A 160 mV Robust Schmitt Trigger Based Subthreshold SRAM," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 10, pp. 2303–2313, Oct. 2007.
- [2] I. J. Chang, J.-J. Kim, S. P. Park, and K. Roy, "A 32 kb 10T Sub-Threshold SRAM Array With Bit-Interleaving and Differential Read Scheme in 90 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 2, pp. 650–658, Feb. 2009.
- [3] T. H. Kim, J. Liu, J. Keane, and C. H. Kim, "A high-density subthreshold SRAM with data-independent bitline leakage and virtual ground replica scheme," in *Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International*, 2007, pp. 330–606.
- [4] B. H. Calhoun and A. Chandrakasan, "A 256kb sub-threshold SRAM in 65nm CMOS," in *Solid-State Circuits Conference, 2006. ISSCC 2006. Digest of Technical Papers. IEEE International*, 2006, pp. 2592–2601.
- [5] G. K. Reddy, K. Jainwal, J. Singh, and S. P. Mohanty, "Process variation tolerant 9T SRAM bitcell design," in *Quality Electronic Design (ISQED), 2012 13th International Symposium on*, 2012, pp. 493–497.
- [6] Ali Valaee, Asim J. Al-Khalili, "SRAM Read-Assist Scheme for High Performance Low Power Applications" in *International SoC Design Conference (ISOCC) on*, 2011, pp. 179-182.
- [7] S. Yoshimoto, M. Terada, S. Okumura, T. Suzuki, S. Miyano, H. Kqwaguchi and M. Yoshimoto, "A 40-nm 0.5-V 20.1- μ W/MHz 8T SRAM with Low-Energy Disturb Mitigation Scheme," in *IEEE Symposium on VLSI Circuits Digest of Technical Papers on*, 2011, pp. 72-73.
- [8] Atsushi Kawasumi, Toshikazu Suzuki, Shinich Moriwaki and Shinji Miyano, "Energy Efficiency Degradation Caused by Random Variation in Low-Voltage SRAM and 26% Energy Reduction by Bitline Amplitude Limiting (BAL) Scheme," in *IEEE Asian Solid-State Circuits Conference on*, 2011, pp. 165-168.
- [9] Mohammad Sharifkhani, Manoj Sachdev, "A Low Power SRAM Architecture Based on Segmented Virtual Grounding," in *International symposium on Low Power Electronics and Design (ISLPED) on*, 2006, pp. 256-261.
- [10] A. Kawasumi, Y. Takeyama, O. Hirabayashi, K. Kushida, F. Tachibana. Y. Niki, S. Sasaki and T. Yabe, "Energy Efficiency Deterioration by Variability in SRAM and Circuit Techniques for Energy Saving without Voltage Reduction," in *IC Design & Technology (ICICDT), 2012 IEEE International Conference on*, 2012.
- [11] Mohammed Shareef I, Pradeep Nair, Bharadwaj Amrutur, "Energy Reduction in SRAM using Dynamic Voltage and Frequency Management," in *2008 21st International Conference on VLSI Design on*, 2008, pp. 503-508.